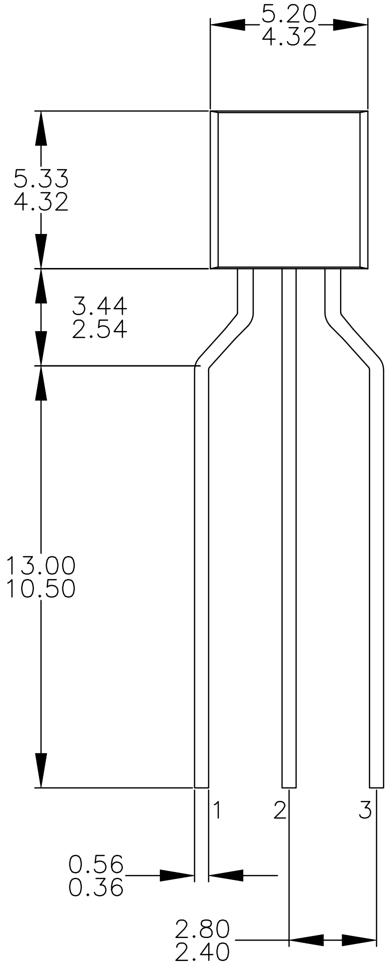
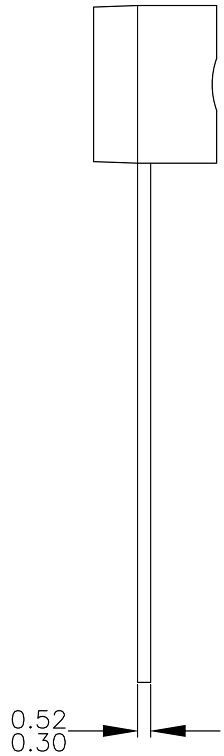
REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JUL.5'96	JT/CB
2	RDRW FR NATIONAL TEMPLATE TO STD FSC MKT DWG TEMPLATE; CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR $\frac{2.667}{2.413}$ TO $\frac{2.80}{2.40}$; CHG STRAIGHT LD LEN FR $\frac{13.00}{11.61}$ TO $\frac{13.00}{10.50}$; CHG MOLD BODY HT FR $\frac{4.699}{4.316}$ TO $\frac{5.33}{4.32}$; CHG MOLD BODY WD FR $\frac{4.699}{4.318}$ TO $\frac{5.20}{4.32}$; ADD PKG THICKNESS DIM; CHG PKG BOT TO LD SURF DIM FR $\frac{2.413}{2.133}$ TO $\frac{2.66}{2.13}$; REMOVE LD SURFACE TO MOLDED SURFACE DIM; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD BENDED LD OVERALL LEN DIM $\frac{3.44}{2.54}$; CHG LD WD FR $\frac{0.508}{0.355}$ TO $\frac{0.56}{0.36}$; CHG LD THICKNESS FR $\frac{0.483}{0.304}$ TO $\frac{0.52}{0.30}$; ADD NOTES SECTION.	26MAR2008	JC/FSCP

APPROVED
July-14-2008





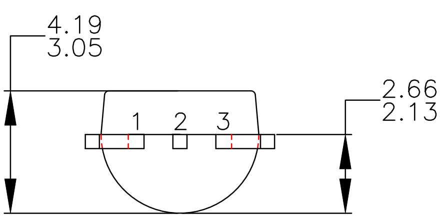
NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO−92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M−1994.
D) TO−92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P − BIPOLAR	E − EMITTER	D − DRAIN
F − JFET	B − BASE	S − SOURCE
M − DMOS	C − COLLECTOR	G − GATE



E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT−ZA03FREV2.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	01APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

FAIRCHILD SEMICONDUCTOR™

3LD,TO−92,MOLDED 0.200 IN LINE SPACING LD FORM(J61Z OPTION)

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	1:1	N/A	MKT−ZA03F	2

FORMERLY: N/A SHEET : 1 OF 1